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PTO - 1449		Applicant(s): Stefan HÖRETH	
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UNITED STATES PATENT DOCUMENTS

Exam. Initials	Ref. No.	Document Number	Date	Inventor(s)	Class	Filing Date

FOREIGN PATENT DOCUMENTS

Exam. Initials	Ref. No.	Document Number	Date	Country or Office	Class	Translation

OTHER DOCUMENTS (INCL. TITLE, AUTHOR, DATE, PAGES, ETC)

Exam. Initials	Ref. No.	
<i>je</i>	CA	Satyanarayana J.J. et al, "Systematic Analysis of Bounds on Power Consumption in Pipelined and Non-Pipelined Multipliers", IEEE Computer Society Press, October 7, 1996, pages 492-499.
<i>je</i>	CB	Bobba S., et al. "Estimation of Maximum Switching Activity in Digital VLSI Circuits" IEEE August 3, 1997, pages 1130-1133.
<i>je</i>	CC	Bhanja S., et al. "Switching Activity Estimation of Large Circuits Using Multiple Bayesian Networks", Proceedings of the 15 th International Conference on VLSI Design. IEEE Computer Society pages 187-192.

Examiner:	<i>Jessica Lee</i>	Date: 6/9/05
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